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Improved Grid Synchronization Algorithm for DG System using DSRF PLL under Grid disturbances

R.Godha[1] Ch.V.S.S.Sailaja[2] K.V.Ramana Murthy[3]
PG Scholor EEE,VCE
Associate Professor EEE,VCE
Professor EEE,VCE

Abstract—
Distributed Generation (DG) System is a small scale electric power generation at or near the user's facility as opposed to the normal mode of centralized power generation. In order to ensure safe and reliable operation of power system based on DS, grid synchronization algorithm plays a very important role. This paper presents a Double Synchronous Reference Frame (DSRF) phase locked loop (PLL) based on synthesis circuit for grid synchronization of distributed generation (DG) system under grid disturbances aimed to provide an estimation of the angular frequency and both the positive and negative sequences of the fundamental component of an unbalanced three-phase signal. The design of this PLL is based on a complete description of the source voltage involving both positive and negative sequences in stationary coordinates and considering the angular frequency as an uncertain parameter.

Keywords- Grid synchronization, phase locked loop, power quality, grid disturbances, positive and negative sequence detection, synthesis circuit, adaptive control, frequency estimation.

I. INTRODUCTION

The power generation systems based on renewable energy systems are distributed near the user's facility. These Distributed Generation (DG) systems need to be controlled properly in order to ensure sinusoidal current injection into the grid. However, they have a poor controllability due to their intermittent characteristics [3]. The major issue associated with DG system is their synchronization with utility voltage vector [4]. Henceforth the study of grid synchronization algorithms is essential.

Few of the earliest known synchronization algorithms include Zero Crossing Detectors (ZCDs). The performance of ZCDs is badly affected by power quality problems, especially in the case of weak grid. The use of Phase Locked Loops (PLLs) for grid synchronization has shown much better results as discussed in [5]. The Linear PLL is mainly used to detect phase for single phase supply. For balanced three phase supply, Synchronous Reference Frame (SRF) PLL is used. But it is found that this PLL fails to detect the phase for unbalanced supply [6]. Hence Decoupled Double Synchronous Reference Frame (DDSRF) PLL was proposed to deal with unbalanced grid conditions like voltage unbalance [7]. DDSRF PLL can detect the positive sequence phase angle in such conditions. Double Synchronous Reference PLL based on synthesis circuit was proposed in [6] which is more frequency adaptive and can be easily implemented.

This paper presents a Double Synchronous Reference Frame (DSRF) PLL (based on synthesis circuit) for grid synchronization of DG system under grid disturbances. Due to flexible in characteristics, DSRF PLL can accurately detect the phase irrespective of the grid conditions along with decoupling of positive and negative sequence components. Further, it demonstrates how the PLLs can track the phase angle during some of the major abnormal grid conditions like voltage unbalance, line to ground fault and voltage sag etc. The superiority of DSRF PLL over SRF PLL is well illustrated by the simulations results obtained from MATLAB/SIMULINK environment.

This paper also presents an algorithm to implement a PLL, which is able to provide an estimation of the angular frequency and both the positive and negative sequences of the fundamental component of an unbalanced three-phase signal. These sequences are provided in fixed -reference-frame coordinates. The synchronization process in the UH-PLL is based on the detection of the fundamental frequency [15]–[17].

II. ANALYSIS OF SRF PLL

A synchronous Reference Frame PLL (SRF PLL) is mainly used for tracking the phase angle in case of 3-phase signals which uses ***Park's Transformation*** of a 3 phase signal as the Phase Detector (PD). Fig.1 depicts the block diagram of a SRF PLL in which v_a , v_b, v_c are the components of a 3 phase signal. First block in the Fig.1 is ***Clarke's***

Transformation which translates a three-phase voltage vector from the *abc* natural reference frame to the αβ stationary reference frame. The second block is the ***Park's Transformation*** which translates the αβ stationary reference frame to rotating frame. A ***Proportional Integrator (PI)*** controller is used as loop filter.

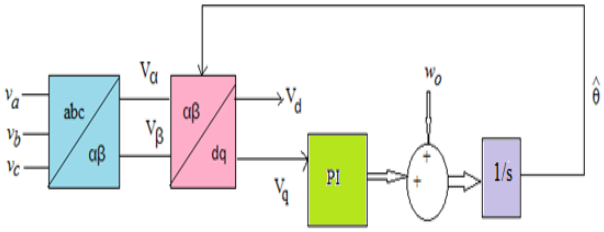


Fig.1 Schematic of SRF PLL

The SRF PLL can be mathematically described by the following equations [6]:-

Under ideal utility conditional, i.e., neither harmonic distortion nor unbalance, the d- and q-axis component can be express by:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} \begin{bmatrix} \cos\theta^{\wedge} & \sin\theta^{\wedge} \\ -\sin\theta^{\wedge} & \cos\theta^{\wedge} \end{bmatrix} = \begin{bmatrix} U\cos\theta \\ U\sin\theta \end{bmatrix} = \begin{bmatrix} U\cos(\theta - \theta^{\wedge}) \\ U\sin(\theta - \theta^{\wedge}) \end{bmatrix} \quad (1)$$

Where θ and $\theta^{\wedge}$ represent the phase of input signal and output of PLL respectively; U is the amplitude of input signal, V_d, V_q are the d- and q-axis component. Under unbalance utility conditions (without voltage harmonics), the voltage vector can be generically expressed as:

$V = V_+ + V_- + V_0$

Where subscripts +, – and 0 define the vector for the positive, negative and zero sequence components. Using Clarke's transformation, the utility voltage vector is given by:

$$V_{\alpha\beta} = \begin{bmatrix} U_+\cos\theta_+ + U_-\cos\theta_- \\ U_+\sin\theta_+ + U_-\sin\theta_- \end{bmatrix} \quad (2)$$

By Park's transformation

$$V_{dq} = T_{dq/\alpha\beta}\, V_{\alpha\beta} = \begin{bmatrix} U_+\cos(\theta_+ - \theta^{\wedge}) + U_-\cos(\theta_- - \theta^{\wedge}) \\ U_+\sin(\theta_+ - \theta^{\wedge}) + U_-\sin(\theta_- - \theta^{\wedge}) \end{bmatrix} \quad (3)$$

Where ω is the angular frequency of voltage vector and $\theta^{\wedge} \approx \theta_+ = -\theta_- = \omega t$ in steady state.

So if the conventional SRF PLL is used during unbalanced grid conditions the second harmonic ripples are so high that makes it difficult to get the information of phase angle and amplitude.

III. ANALYSIS OF DSRF PLL

From [6] the Dual SRF PLL (DSRF PLL) is a combination of two conventional SRF-PLLs. These two frames are separated by a synthesis circuit. The voltage vector is decomposed into positive and negative sequence vectors and these components are denoted by V+ and V- respectively as shown in Fig. 2. As shown in Fig. 4, the α - and ß-axis components both contain the information of the positive sequence and negative sequence which makes it difficult to detect the positive sequence component. The two PLLs work independently, rotating with positive direction and negative direction respectively and detect the positive sequence and negative sequence simultaneously.

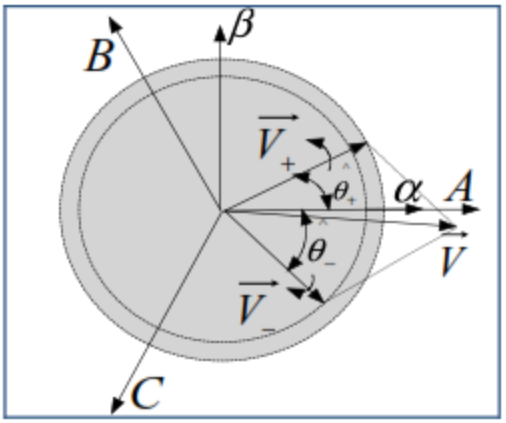


Fig. 2 Voltage Vector Decomposition (unbalanced voltage)

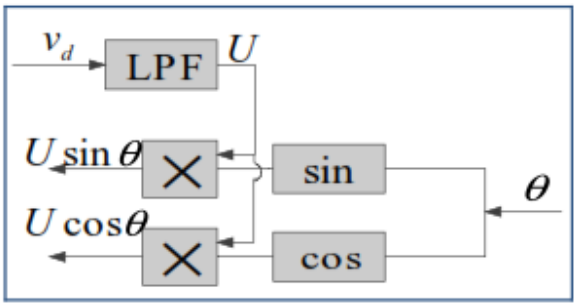


Fig. 3 Synthesis Circuit used in DSRF PLL

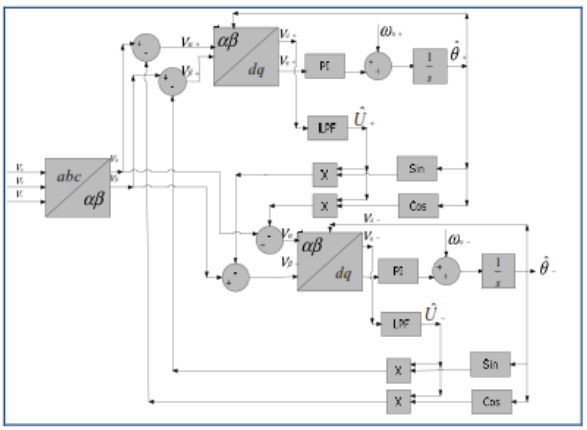


Fig. 4 Dual SRF PLL structure

The d-axis component from the Park's transformation is fed to the synthesis circuit. This signal is actually the voltage amplitude in steady state. The synthesis circuit consists of a Low Pass Filter (L.P.F.), two multipliers, and two orthogonal trigonometric

functions as shown in Fig. 3. The main objective of the orthogonal functions is to create orthogonal and in-phase signals with respect to the input signal multiplying them with the amplitude. These signals are used as decoupling signals as shown in the Fig. 4.

The two PLLs are required to detect the positive and negative sequence at the same time. The signals generated by the synthesis circuit are used as feedback for the unbalanced input signal. The input to the Park's transformation, V_α and V_β is the difference of actual V_α and V_β and the generated signals from the other PLL. As the process goes on the input to the PLL cleans up and the distortion at the output is cancelled. The positive sequence is detected by the PLL with ω_{0+}as the initial angular frequency and the negative sequence is detected by the one with ω_{0-}as the initial angular frequency. The behavior of DSRF PLL is explained by the equation given below [6].

In the initial state, v_d is zero, $\theta\hat{}$ is $\omega_0 t$, the output of synthesis circuit are all equal to zero that means decoupling circuit has no effect and each PLLs contains both positive sequence and negative sequence information. In rotating reference frame rotating with positive direction, the Park's transformation output is:

$$\begin{bmatrix} V_{d+} \\ V_{q+} \end{bmatrix} = U_+ \begin{bmatrix} \cos(\theta_+ - \hat{\theta}_+) \\ \sin(\theta_+ - \hat{\theta}_+) \end{bmatrix} + U_- \begin{bmatrix} \cos(\theta_- - \hat{\theta}_-) \\ \sin(\theta_- - \hat{\theta}_-) \end{bmatrix} \quad (4)$$

$\hat{\theta}_+$ is $\omega_{0+}t$ at initial state, where ω_{0+} is approximate the centre angular frequency of positive sequence component.

Then (5) becomes

$$\begin{bmatrix} V_{d+} \\ V_{q+} \end{bmatrix} = \begin{bmatrix} U_+ + U_- \cos(-2\omega_{0+}t) \\ U_- \sin(-2\omega_{0+}t) \end{bmatrix} \quad (5)$$

There is 2ω ripple including in the d-axis component, so a low-pass filter (LPF) is need to attenuate ripple and help the PLL to get stable. The LPF can be defined as:

$$\text{LPF}(s) = \frac{\omega_c}{s+\omega_c}$$

Where ω_c determines the cut-off frequency of LPF.

In order to analyze the behavior of proposed PLL. The state equations can be derived as

$$\begin{cases} \dot{x}_1 = \omega_c (U_+ - x_1 + (U_- - x_2)\cos(\theta_+ - \theta_-)) \\ \dot{x}_2 = \omega_c (U_- - x_2 + (U_+ - x_1)\cos(\theta_+ - \theta_-)) \end{cases} \quad (6)$$

Where $\begin{cases} \dot{x}_1 = U_+ \\ \dot{x}_2 = U_- \end{cases}$

When the state variables get into steady state, there will be $x_1 = U_+$ and $x_2 = U_-$ .That is, the d-axis component will converge to input voltage vector amplitude after some time, and synthesis circuit start to output decoupling signals. At last the input of each PLL will be:

$$\begin{cases} V_{\alpha+} = V_\alpha - U_- \cos\theta_- = U_+ \cos\theta_+ \\ V_{\beta+} = V_\beta - U_- \sin\theta_- = U_+ \sin\theta_+ \end{cases} \quad (7)$$

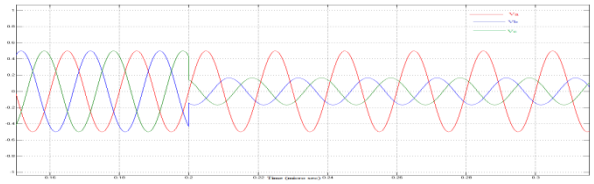
And

$$\begin{cases} V_{\alpha-} = V_\alpha - U_+ \cos\theta_+ = U_- \cos\theta_- \\ V_{\beta-} = V_\beta - U_+ \sin\theta_+ = U_- \sin\theta_- \end{cases}$$

IV. RESULTS AND DISCUSSIONS

A. *SRF PLL Under Unbalanced Three Phase Voltage*

The results obtained from simulation of SRF PLL for unbalanced input voltage are shown in Fig. 5. Fig. 5 (a) shows the 3 phase unbalanced input fed to an SRF PLL such that phase a magnitude is greater than the other 2 phases. As described in (4) the d and q axis voltages are not constant, rather contains second harmonic ripples. Fig. 5 (b) shows these second harmonic components in d axis and q axis voltages. This sinusoidal nature in q axis voltage affects the output of PI controller and generates sinusoidal error signal and hence sinusoidal angular frequency (at central frequency ω_0 which is 100 π in this case). From Fig.5 (c), it can be seen that, the detected phase obtained by the time integration of angular frequency is not perfectly triangular but rather contains sinusoidal variations.



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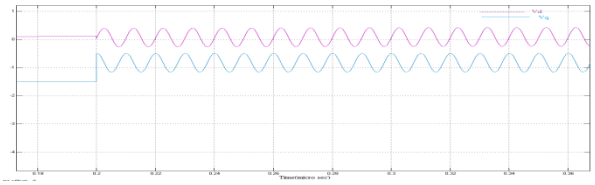

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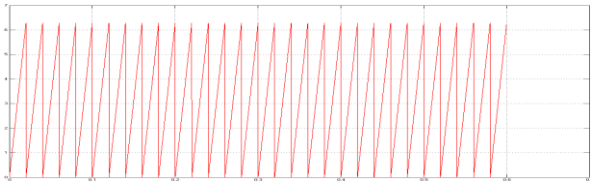
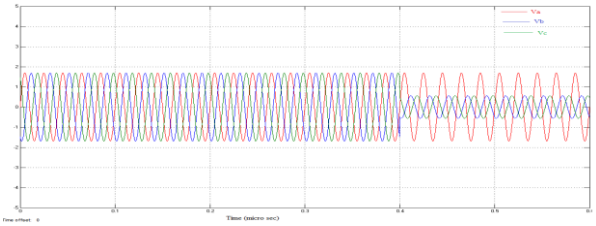


(c)

Fig.5 Simulation Results for SRF PLL under unbalanced grid conditions. (a) grid voltage waveforms (b) d-q components of grid voltage (c) detected phase angle.

B. Dynamic Response of DSRF PLL Under unbalaced Grid Voltages

The dynamic responses obtained from simulation for DSRF PLL under unbalance input voltage are shown in Fig.6. The PI tuning used for these results are Kp =67.5 and Ki =100.



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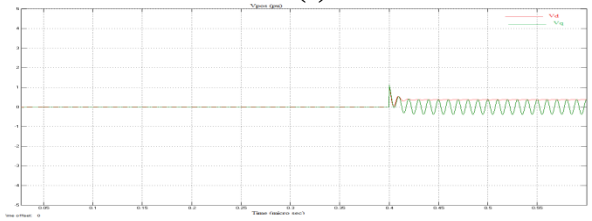

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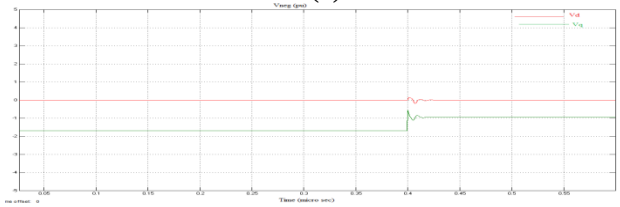

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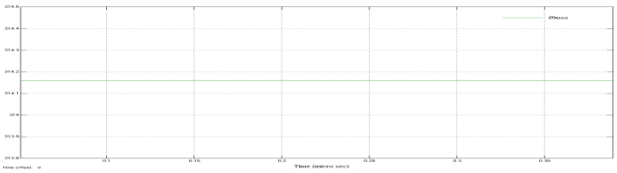

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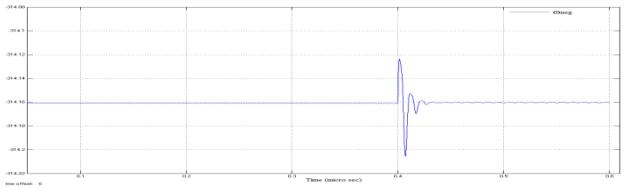

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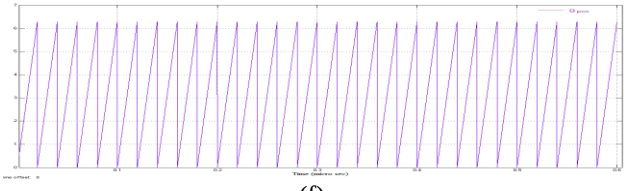
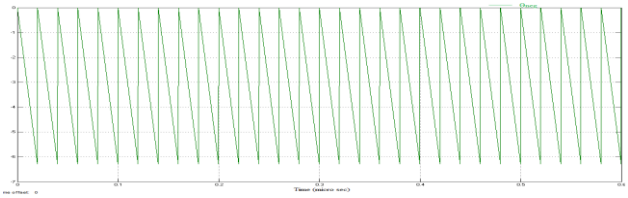


(f)



(g)

Fig. 6 Dynamic response of DSRF PLL under unbalanced grid conditions (a) grid voltage waveforms (b) d and q axis positive sequence component of grid voltage (c) d and q axis negative sequence component of grid voltage (d) detected angular frequency of positive sequence component (e) detected angular frequency of negative sequence component (f) detected phase angle of positive sequence component (g) detected phase angle of negative sequence component.

Fig 6(a) shows a 3-phase signal which is balanced up to time t=0.4 sec and then voltage amplitude of 2 of the phases reduces to 0.5 from their initial value of 1.5. With this kind of input the dynamic responses are observed. The positive and negative sequence components are separately observed in case of DSRF PLL. In Fig 6(b) the d axis voltage of positive sequence component is almost constant both during balanced and unbalanced period and negligible sinusoidal variations are observed during the transient period (from t=0.4 to 0.42 sec). The q axis voltage of the positive sequence component maintains mostly a constant value both in balanced and unbalanced conditions. The transients are observed when there is sudden change in input voltage (at t=0.4 sec). The transient vanishes to give a nearly constant value (nearly at zero) for q axis voltage of positive sequence component.

As shown in Fig 6(c) the d axis voltage of negative sequence component is also almost constant having negligible variations. The q axis voltage of the negative sequence component maintains mostly a constant value both in balanced and unbalanced conditions. The transients are observed when there is sudden change in input voltage (at t=0.4 sec). The transient vanishes to give a nearly constant value (nearly at zero) for q axis voltage of negative sequence component.

In Fig 6(d) the angular frequencies of positive and negative sequence components are both similar to their respective q axis voltages and hence a nearly constant angular frequency is observed for positive and negative sequence components.

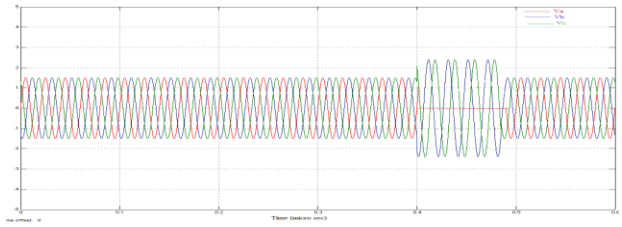
Fig 6(e) shows that the angular frequencies of positive and negative sequence components are both similar to their respective q axis voltages and hence a nearly constant angular frequency is observed for positive and negative sequence components.

In Fig 6(f) for the constant angular frequencies we observe perfectly triangular phase angle detection for positive sequence. The detected phase angle varies linearly every cycle from 0 to 2π for positive sequence.

In Fig 6(g) for the constant angular frequencies we observe perfectly triangular phase angle detection for negative sequence. The detected phase angle varies linearly every cycle from 0 to -2π for negative sequence.

C. Response of DSRF PLL Under Line to Ground fault

The results obtained from simulation for DSRF PLL underline to ground fault are shown in Fig. 7. The PI tuning used for these results are K_p =67.5 and K_i =100.



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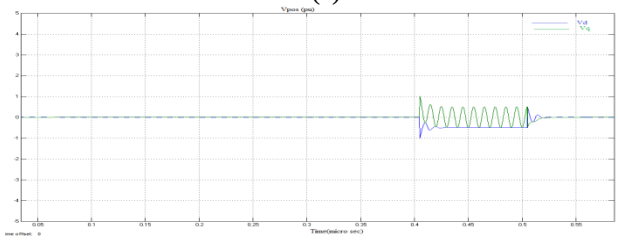

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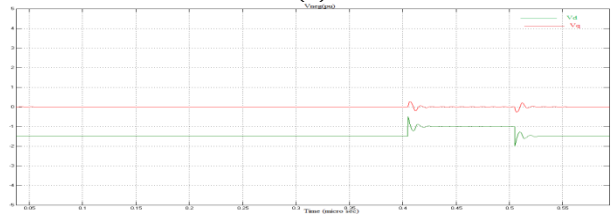

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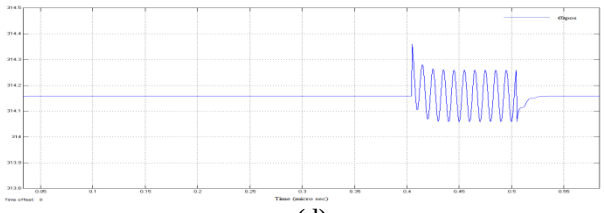

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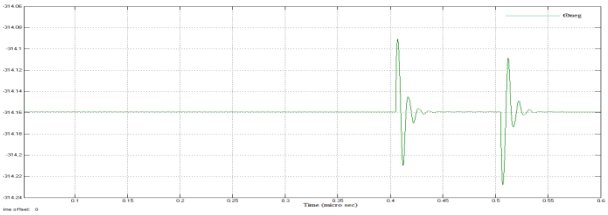

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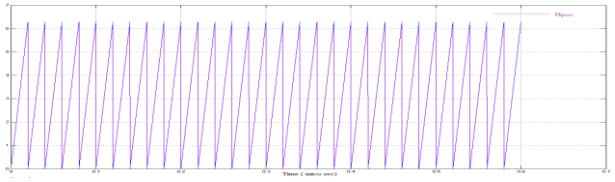

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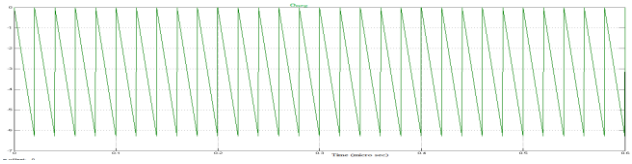


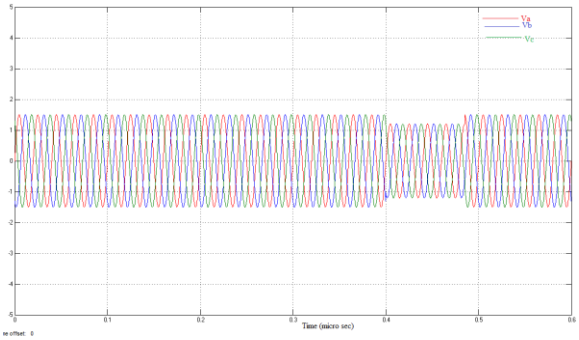
(g)

Fig. 7 Simulation results obtained for DSRF PLL under line to ground fault (a) grid voltage waveforms (b) d axis and q axis positive sequence component of grid voltage (c) d axis and q axis negative sequence component of grid voltage (d) detected angular frequency of positive sequence component (e) detected angular frequency of negative sequence component (f) detected phase angle of positive sequence component (g) detected phase angle of negative sequence component.

Fig. 7(a) shows the input to the system when line to ground fault occurs. The system was initially in balanced condition (having amplitude 1.5V). Line to ground fault occurs at time, t = 0.4sec.At this instant the phase voltage of 2 of the phases increases and remains at an amplitude of 2.4V. The system regains its balanced state at time, t = 0.5 sec. The d axis voltage of positive sequence component shown in Fig. 7(b) is constant at the amplitude of the signals during balanced input. During line to ground fault the d axis voltage reduces and some oscillations with very small amplitude are observed. The d axis voltage for negative sequence component (Fig.7(c)) also maintains its constant value other than very small transients that occur at time t = 0.4 sec and 0.5 sec. The q axis voltages for positive sequence (Fig. 7(b)) and negative sequence (Fig. 7(c)) maintains their near zero value at all Instants, with some oscillations at the instants when switching of voltages occur. The angular frequencies of positive sequence and negative sequence components maintain their constant value at 100 π and -100 π (Fig. 7(d) and Fig. 7(e) respectively).Therefore the detected phase angle is perfectly triangular for both positive (Fig. 7(f)) and negative sequence (Fig. 7(g)).

D. Response of DSRF PLL Under Voltage Sag

The simulation results obtained for DSRF PLL under Voltage sag are shown in Fig. 8.The PI tuning used for these results are K_p = 67.5 and K_I =100.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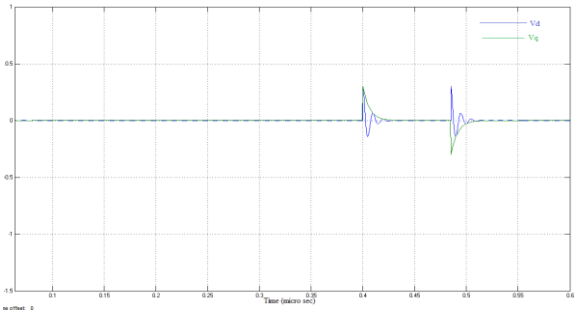
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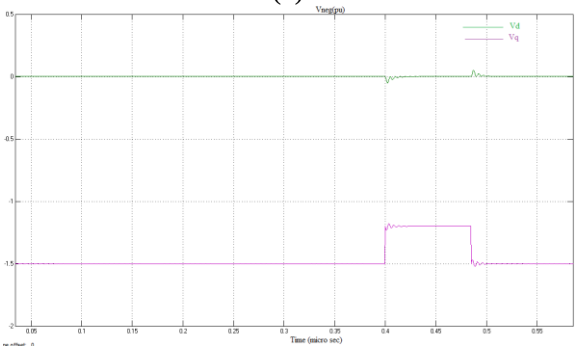
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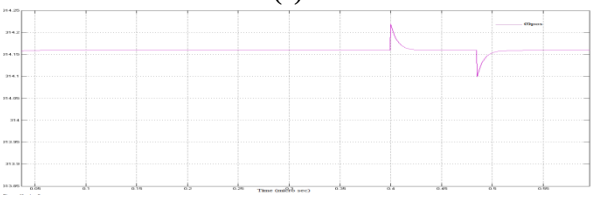
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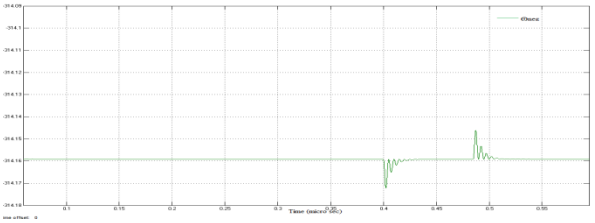
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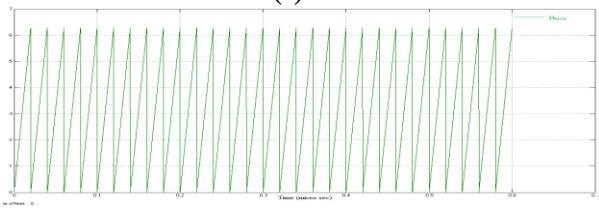
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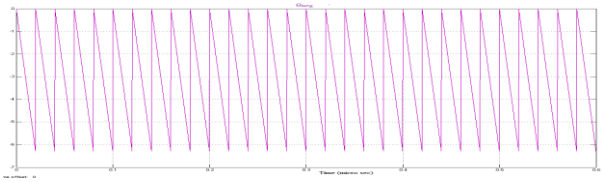
(g)

Fig. 8 Simulation results obtained for DSRF PLL under voltage sag (a) grid voltage waveforms (b) d axis and q axis positive sequence component of grid voltage (c) d axis and q axis negative sequence component of grid voltage (d) detected angular frequency of positive Sequence component (e) detected angular frequency of negative sequence component (f) detected phase angle of positive sequence component (g) detected phase angle of negative sequence component

As shown in Fig. 8(a), voltage sag occurs at time t = 0.3 sec when all the three phases voltages reduces to 0.45V from their initial voltage of 0.5V. The 3 phases regain their original value of 0.5V at time t = 0.4 sec. This kind of sudden reduction is voltage for small period (2 and half cycles in this case) is known as voltage sag.Fig.8 (b) illustrates the d axis voltage of positive sequence component, which is constant at the amplitude of the input signal. In the duration when voltage sag occurs, the d axis voltage remains constant but its value changes to the new amplitude. Similarly as shown in Fig. 8(c) the d axis voltage of negative sequence component also maintains its constant zero value. The q axis voltage of positive sequence component remains constant at a value very close to zero and some slight transients are observed at the time of switching (Fig. 8 (b). The same holds good for q axis voltage of negative sequence component which remains constant at zero in both the periods (Fig. 8(c)). As q axis voltages are constant the corresponding angular frequency for both positive and negative components maintains their constant value at 100 π and -100 π (Fig. 8(d) and Fig. 8(e)).The detected phase for both the sequence components is perfectly triangular because of the constant angular frequency observed.

V. CONCLUSIONS

The paper presents the performance of Dual Synchronous Reference Frame (DSRF) PLL for phase detection under grid disturbances. The grid disturbances include, voltage unbalance, line to ground fault and voltage sag. From the above discussions, one can observe that, the studied DSRF PLL can accurately detect the phase irrespective of the grid conditions. Moreover, the DSRF PLL can also decouple the positive and negative sequence components of grid voltages in order to ensure sinusoidal current injection into the Grid. Further, the obtained results clearly show that the DSRF PLL gives better response to track the positive sequence component over conventional SRF PLL which fails to track the phase angle whenever there is an unbalance in the grid. On the other hand DSRF PLL properly handles the abnormalities and the phase angle is perfectly detected in each case. The improvement in this study will be enhanced by implementing the DSRF PLL in digital platform using FPGA in the future work.

REFERENCES

[1.] R. Teodorescu and F. Blaabjerg, "Flexible control of small wind turbines with grid failure detection operating in stand-alone and grid-connected mode," IEEE Trans. Power Electron., vol. 19, no. 5, pp.1323–1332, Sep. 2004.

[2.] Z. Chen, "Compensation schemes for a SCR converter in variable speed wind power systems," IEEE Trans. Power Delivery, vol. 19, pp. 813-821, Apr. 2004.

[3.] F. Blaabjerg, Z. Chen and S. Kjaer, "Power Electronics as Efficient Interface in Dispersed Power Generation Systems," *IEEE Trans. PowerElectron.*, vol. 19, no. 5, pp. 1184-1194, Sep. 2004.

[4.] A. Timbus, R. Teodorescu, F. Blaabjerg and M. Liserre, "Synchronization Methods for Three Phase Distributed Power Generation Systems. An Overview and Evaluation," in Proc. 2005 Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36,pp. 2474-2481.

[5.] Francisco D. Freijedo, Jesus Doval-Gandoy, Oscar Lopez, Carlos Martinez-Penalver, Alejandro G. Yepes, Pablo Fernandez-Comesana, Andres Nogueiras, JanoMalvar, Nogueiras, Jorge Marcos and AlfonsoLago, "Grid-Synchronization Methods for Power Converters," Proc. Of IEEE, pp. 522 – 529, 2009.

[6.] FANG Xiong, WANG Yue, LI Ming, WANG Ke and LEI Wanjun, "A Novel PLL for Grid Synchronization of Power Electronic Converters inUnbalanced and Variable-Frequency Environment," Proc. of IEEE International Symposium on Power Electronics for Distributed Generation Systems: pp. 466-471, 2010.

[7.] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos and D. Boroyevich, "Decoupled Double Synchronous Reference Frame PLL for Power Converters Control," *IEEE Transactions on, PowerElectronics*, vol. 22, pp. 584-592, 2007.

[8.] J. Svensson, "Synchronisation methods for grid-connected voltage source converters," Proc. Inst. Electr. Eng.—Gener. Transm. Distrib., vol. 148, no. 3, pp. 229–235, May 2001.

[9.] M. Karimi-Ghartemani and M. Iravani, "A method for synchronization of power electronic converters in polluted and variable-frequency environments," IEEE Trans. Power Syst., vol. 19, no. 3, pp. 1263–1270, Aug. 2004.

[10.] L.R. Limongi, R. Bojoi, C. Pica, F. Profumo, A. Tenconi, "Analysis and Comparison of Phase Locked Loop Techniques for Grid Utility Applications" Proc. IEEE Power Conversion Conference PCC, 2007, pp. 674-681.

[11.] R. M. Santos Filho, P. F. Seixas, P. C. Cortizo, L. A. B. Torres, and A. F. Souza, "Comparison of three single-phase PLL algorithms for UPS applications" IEEE Trans. on Industrial Electronics, Vol. 55, No. 8, pp. 2923-2932, August 2008.

[12.] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos and D. Boroyevich, "Decoupled Double Synchronous Reference Frame PLL for Power Converters Control," Power Electronics, IEEE Transactions on, vol.22, pp. 584-592, 2007.

[13.] G. Escobar, M.F. Martinez-Montejano, A.A. Valdez, P.R. Martinez and M. Hernandez-Gomez, "Fixed-Reference-Frame Phase-Locked Loop for Grid Synchronization Under Unbalanced Operation," IEEE Trans. on Ind.Electron., Vol. 58, Issue 5, pp. 1943-1951, May 2011.

[14.] D. Yazdani, M. Mojiri, A. Bakhshai and G. Joos, "A Fast and Accurate Synchronization Technique for Extraction of Symmetrical Components, "IEEE Trans. on Power Electron., Vol. 24, Issue 3, pp. 674-684, March2009.